IN THE CLAIMS

1. (Original) A method of making a semiconductor device comprising:

providing a substrate having a source region and a drain region, each of the source region and the drain region includes a plurality of sections;

creating a shallow trench isolation (STI) region between each two sections of the source region and between sections of the drain region;

forming a gate stack on the substrate;

implanting the substrate to create the source region and the drain region; and

forming a tensile stress inducing layer over the substrate , the tensile stress inducing layer covering the STI regions, the source region, the drain region, and the gate stack.

2. (Original) The method of claim 1 further comprising:

forming a silicide layer over the source region, the drain region, and the gate stack prior to forming the tensile stress inducing layer over the substrate.

3. (Original) The method of claim 1 wherein the gate stack includes a gate electrode layer formed on a gate dielectric layer.

4. (Original) The method of claim 1 further comprising:

creating contacts to the source region, the drain region, and the gate stack.

5. (Original) The method of claim 1 wherein the STI regions have surfaces that are below the surfaces of the substrate.

6. (Original) The method of claim 1 wherein the tensile stress inducing layer is a nitride etch stop layer.

7. (Original) The method of claim 1 wherein the tensile stress inducing layer introduces tensile stress into a channel region in the substrate.

8. (Original) The method of claim 1 wherein the substrate is one of a silicon comprising substrate, a monocrystalline silicon substrate, a germanium silicon substrate, and silicon on insulator substrate.

9. (Original) The method of claim 1 further comprises continuing the forming of the tensile stress inducing layer over the substrate until the tensile stress inducing layer reaches a thickness between about 25 nm and about 150 nm.

10. (Original) The method of claim 1 wherein the tensile stress inducing layer introduces a tensile stress ranging between about 200 mega Pascal and about 300 mega Pascal into the substrate.

11. (Original) The method of claim 1 wherein the tensile stress inducing layer conforms to exposed surfaces on the substrate.

12. (Currently Amended) A method of creating tensile stress in a silicon substrate comprising:

providing a substrate;

creating a shallow trench isolation (STI) region between sections of the substrate;

forming a source region and a drain region in said substrate for a semiconductor device, wherein at least two section selected from the plurality of sections of the substrate form one source region and at least two section selected from the plurality of sections of the substrate form one drain region; and

forming a tensile inducing layer over the substrate, the tensile inducing layer being an insulation material capable of causing tensile stress in the substrate.

13. (Currently Amended) The method of claim 12 further comprises, forming a gate stack between each pair of a source and a drain regions wherein the gate stack is continuous and not divided into sections ~~wherein at least two sections selected from the sections of the substrate form a source region and a drain region for a semiconductor device~~.

14. (Original) The method of claim 12 wherein the tensile stress introduced into the substrate by the tensile inducing layer forms a channel region of a semiconductor device in the substrate.

15. (Original) The method of claim 12 further comprising:

forming a gate stack on the substrate; and

implanting source and drain materials into the substrate to create the source region and the drain region;

wherein the tensile inducing layer is formed over the substrate, over the gate stack, and over the source and drain regions.

16. (Original) The method of claim 15 wherein the gate stack includes a gate electrode layer and a gate dielectric layer.

17. (Original) The method of claim 15 further comprising:

creating contacts to the source region, the drain region, and the gate stack.

18. (Original) The method of claim 12 wherein the STI regions have surfaces that are below the surfaces of the substrate.

19. (Original) The method of claim 12 wherein the tensile inducing layer is a nitride etch stop layer.

20. (Original) The method of claim 12 wherein the substrate is one of a silicon comprising substrate, a monocrystalline silicon substrate, a germanium silicon substrate, and silicon on insulator substrate.

21. (Original) The method of claim 12 further comprises continuing the forming of the tensile inducing layer over the substrate until the tensile inducing layer has a thickness between about 25 nm and about 150 nm.

22. (Original) The method of claim 12 wherein the tensile inducing layer introduces a tensile stress ranging between about 200 mega Pascal and about 300 mega Pascal into the substrate.

23. (Original) The method of claim 12 wherein the tensile inducing layer conforms to exposed surfaces on the substrate.

24. (Withdrawn) A semiconductor device comprising:

a substrate having a source region and a drain region, each of the source region and the drain region includes a plurality of separated sections;

a shallow trench isolation (STI) region formed between each two separated sections of the source region and between each two separated sections of the drain region;

a gate stack formed on the substrate; and

a tensile stress inducing layer formed over the substrate, the tensile stress inducing layer covering the STI regions, the source region, and the drain region.

25. (Withdrawn) The semiconductor device of claim 24 further comprising:

a silicide layer formed over the source region, the drain region, and the gate stack and wherein the tensile stress inducing layer formed over the substrate is formed over the silicide layer.

26. (Withdrawn) The semiconductor device of claim 24 wherein the gate stack includes a gate electrode layer and a gate dielectric layer.

27. (Withdrawn) The semiconductor device of claim 24 further comprising:

contacts interconnected to the source region, the drain region, and the gate stack.

28. (Withdrawn) The semiconductor device of claim 24 wherein the STI regions have surfaces that are below the surfaces of the substrate.

29. (Withdrawn) The semiconductor device of claim 24 wherein the tensile stress inducing layer is a nitride etch stop layer.

30. (Withdrawn) The semiconductor device of claim 24 wherein the tensile stress inducing layer introduces tensile stress into a channel region in the substrate.

31. (Withdrawn) The semiconductor device of claim 24 wherein the substrate is one of a silicon comprising substrate, a monocrystalline silicon substrate, a germanium silicon substrate, and silicon on insulator substrate.

32. (Withdrawn) The semiconductor device of claim 24 wherein the tensile stress inducing layer has a thickness between about 25 nm and about 150 nm.

33. (Withdrawn) The semiconductor device of claim 24 wherein the tensile stress inducing layer introduces a tensile stress ranging between about 200 mega Pascal and about 300 mega Pascal into the substrate.

34. (Withdrawn) The semiconductor device of claim 24 wherein the tensile stress inducing layer is a conformal layer.

35. (New) A method of making a semiconductor device comprising:

forming a source region and a drain region in a substrate;

forming a gate stack on the substrate;

enhancing tensile stress of the semiconductor device by forming each of the source region and the drain region to includes a plurality of narrow parallel sections, wherein each two narrow parallel sections are separated by a shallow trench isolation (STI) region, and by forming a tensile stress inducing layer over the substrate , the tensile stress inducing layer covering the STI regions, the source region, the drain region, and the gate stack.

36. (New) The method of claim 35 wherein the gate stack includes a gate electrode layer formed on a gate dielectric layer and wherein the gate stack is a continuous section.

37. (New) The method of claim 35 wherein the STI regions have surfaces that are below the surfaces of the substrate.